ZnO nanowire network transistor fabrication on a polymer substrate by low-temperature, all-inorganic nanoparticle solution process

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All-solution processed, low-temperature zinc oxide nanowire network transistor fabrication on a polymer substrate was demonstrated. This simple process can produce high resolution metal electrode transistors with inorganic semiconductor nanowire active material in a fully maskless sequence, eliminating the need for lithographic and vacuum processes. The temperature throughout the processing was under 140 °C, which will enable further applications to electronics on low-cost, large-area flexible polymer substrates. © *2008 American Institute of Physics*.
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The development of liquid solution based material processing has been stimulated by significant recent interest and development in direct patterning of functional materials as alternatives to the conventional microfabrication based on photolithography and vacuum deposition processes, specifically in the area of low-cost flexible electronics.[1,2] Especially, metal nanoparticle (NP) solution based direct patterning techniques are receiving great attention for high performance electronics.[3–6,9] This approach exploits the dramatic melting temperature depression of the metal NP for the low-temperature direct metal micro-/nanofabrication process.

However, this NP based direct patterning technique is mainly applied to inkjet printing and the best resolution is limited to 20–50 μm by the nozzle diameter, the statistical variation of the droplet flight, and spreading on the substrate. Among direct patterning techniques, nanoimprinting has demonstrated the highest resolution (even submicron) but has mostly been limited to the fabrication of conducting polymer[7,8] structures, which, however, has inferior electrical performance.[2] Very few direct metal imprinting techniques[9] have been demonstrated. In addition, most solution processible semiconductors today are *p*-type organic materials, even though most organic semiconductors have poor air stability and low mobility compared to inorganic semiconductors. Since most conventional organic semiconducting polymers have low resistance to the air environment due to oxidation, their operation has mostly been limited in the vacuum or inert environment. Air-stable semiconducting polymer has been developed, but it still has a low hole mobility and exhibits slow degradation of electrical performance in the air environment.[10] Direct synthesis of inorganic semiconductor by gas-phase approaches such as metal organic chemical vapor deposition,[11] chemical vapor transport,[12] and pulsed laser deposition[13] can produce high quality air-stable inorganic semiconductor nanowires (NWs). However, these processes face several limitations such as elevated synthesis temperature (450–900 °C), sample uniformity, substrate dependence, and low manufacturing yield. In contrast, aqueous solution approaches are appealing because of the low growth temperatures (<100 °C), potential for scaling up, and straightforward methods of producing high-density arrays of NWs and nanorods.[14] Most of all, they are highly cost effective because they preclude the need for vacuum environment and limited selection of substrates.

In this letter, we demonstrate all-solution processed, low-temperature ZnO NW transistor fabrication process on polymer substrates by combining two different NP (Au and ZnO) based solution processes—Au NP direct nanoimprinting and the ZnO NW synthesis on ZnO NP seeds. The ZnO NW network transistor (NWNT) fabrication process consists of two main steps: (i) source-drain electrode fabrication by the direct nanoimprinting of Au NPs and (ii) hydrothermal ZnO NW growth from ZnO NP seeds in aqueous ZnO precursors. Both steps are low-temperature (T_{max} < 140 °C), NP based solution processes. These characteristics make this technique directly applicable to low-cost, solution processed electronics on inexpensive polymer substrates.

As a first step, the source-drain electrode fabrication process by the direct nanoimprinting of metallic NPs is illustrated in Figs. 1(a)–1(c). Self-assembled monolayer (SAM) protected gold NP solution is dispensed on a dielectric/gate

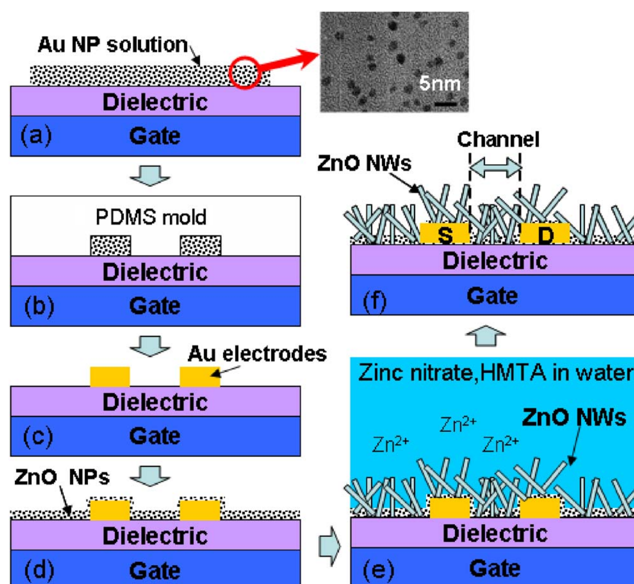

FIG. 1. (Color online) Schematic illustration of the ZnO NW network FET fabrication process. Removal of a mold and induced Au NP melting on a hot plate at 140 °C. The pictures are not scaled.

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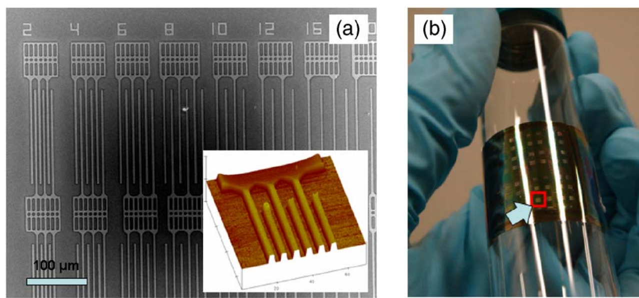

FIG. 2. (Color online) (a) SEM picture and AFM topography image (inset) of transistor electrodes fabricated by direct nanoimprinting of Au NPs on the SiO_2/n^+ Si wafer. (b) A digital photograph of transistor arrays on a PVP/Al/PI flexible substrate. A red square represents an array of 36 transistors.

substrate and imprinted by using a polydimethylsiloxane (PDMS) stamp at low pressure (<40 kPa) and low temperature (80 °C). The dielectric/gate substrates used in this research are a SiO_2/Si wafer (n^+) and a poly(vinyl phenol) (PVP)/Al/polyimide (PI) substrate. After the NP solvent evaporation and cooling, the PDMS stamp is demolded and imprinted metal NP patterns are heated up to 140 °C for 10 min to induce NP melting. SAM protected Au NPs [2–3 nm, Fig. 1(a), inset transmission electron microscopy (TEM) picture] are synthesized through a two-phase reduction method and encapsulated by hexanethiol SAM in an organic solvent (α-terpineol).[6] The melting point of Au NPs is approximately 130–140 °C, which is substantially lower than that of bulk gold due to thermodynamic size effect, as verified by the evolution of electrical resistivity, reflectance, and mass of the Au NP thin film.[15] Moderate heating during the nanoimprinting process allows the NP solution to have a low viscosity and facilitates successful pattern replication with a minimum residual layer. The imprinting processing temperature was optimized at 80 °C to achieve the best filling of the solution into the PDMS stamp.

As a second step, a network of ZnO NWs was synthesized on a substrate with Au source-drain electrodes via a hydrothermal process, as illustrated in Figs. 1(d)–1(f). The solution approach to ZnO NW synthesis[16] was modified in this work. ZnO quantum dots (3–4 nm, Meliorum Technology Inc.) in ethanol were spin coated to form uniform seeds for ZnO NW growth. NWs were grown by immersing the seeded substrate in aqueous solutions containing 25 mM zinc nitrate hydrate [$Zn(NO_3)_2 \cdot 6H_2O$] and 25 mM hexamethylenetetramine ($C_6H_{12}N_4$) at 65–95 °C for 3 h. Finally, the ZnO NWs grown on the substrate were thoroughly rinsed with MilliQ water and dried in air at 120 °C. The ZnO NWNT fabricated in this work has a bottom gate/bottom contact transistor configuration [Fig. 1(f)].

Figure 2(a) shows the atomic force microscope (AFM) topography and the scanning electron microscope (SEM) pictures of the transistor electrode arrays on the SiO_2/n^+ Si wafer by direct nanoimprinting of metal NPs. To demonstrate the applicability for the flexible electronics, the direct nanoimprinted transistor arrays (approximately 400 transistors) were also demonstrated on a PVP/Al/PI flexible substrate and then attached on a curved surface [Fig. 2(b)]. Single or multiple channel electrodes of various channel lengths (2–50 μm) with 300 nm height were fabricated. Very clean and precise short channels were produced by the direct nanoimprinting process. The residual layer of direct nanoimprinted Au NPs is very critical for high performance electronics because it may cause a leakage current. The fluidic property (viscosity and surface tension) control of NP carrier solvent and the conformal PDMS stamp-substrate surface contact facilitate the complete pattern replication with a minimal residual layer. The absence of the residual layer was verified by electrical measurement, AFM scanning, and energy dispersive x-ray analysis. This eliminates the need of additional wet etching of Au NP residues before the usage as the transistor electrodes.

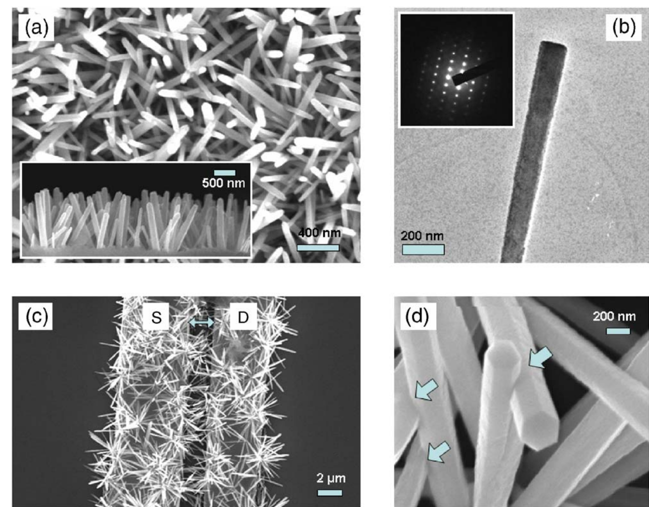

FIG. 3. (Color online) Hydrothermally grown ZnO NWs. (a) SEM top view picture and cross sectional picture (inset). (b) TEM image and SAED (inset) image. (c) SEM picture of ZnO NW network grown on direct nanoimprinted Au electrodes and (d) magnified view. Arrows indicate the junctions between NWs.

The quality of the ZnO NWs synthesized through the hydrothermal process has been characterized by SEM and TEM. The top view and cross sectional images of the ZnO NWs on SiO_2/Si wafer are given in Fig. 3(a). The cross sectional SEM view [Fig. 3(a), inset] suggests that the ZnO NWs directionally grow, deviating by a few degrees from the perpendicular to the substrate direction. Hexagonal NWs of typically 150–300 nm diameters and up to 1–3 μm long grew on the substrates along the c axis of the wurtzite crystal. TEM characterization of individual NWs indicates that they are single crystalline and grow in the [0001] direction [Fig. 3(b): TEM picture, inset, selected area electron diffraction (SAED) pattern]. The actual ZnO NW growth on nanoimprinted electrodes is shown in Fig. 3(c). The ZnO NWs connect the two electrodes through forming complex NW networks whose connectivity can be observed in Fig. 3(d). The initial deposition of the ZnO quantum dot seeds is critical for the NW diameter and growth direction control. Highly oriented and dense ZnO NW arrays could be synthesized from ZnO nanocrystal seeds that were formed from the decomposition of a zinc acetate precursor at 350 °C.[17] However, well ordered vertical NWs are not ideal for the effective electronic path between two planar electrodes. Multiple NWs grew from a single aggregate of ZnO NPs attached to the substrate to form slanted NW forest. These slanted NWs showed more effective channel formation.

The averaged output characteristic and transconductance (g_m) plot of 18 ZnO NWNTs are shown in Fig. 4(a) for 10 μm nanoimprinted channel length. The ZnO NWNT shows n-type accumulation device characteristics working in a depletion mode with I_{on}/I_{off} ratio of 10^4–10^5, sub-

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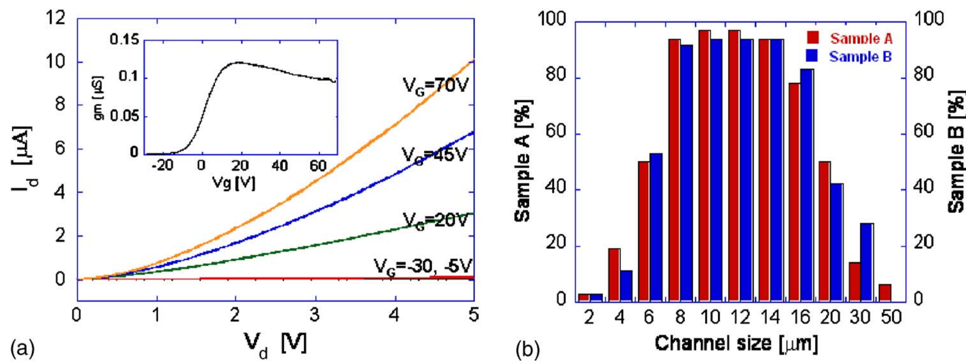

FIG. 4. (Color online) (a) Averaged output characteristics of the 18 ZnO NWNTs with 10 μm channel length. The inset picture represents a transconductance (g_m) plot. (b) Yield statistics of 400 ZnO NWNTs on a SiO_2/n^+ Si wafer (sample A) and a PVP/Al/PI substrate (sample B).

threshold slope of 8 V/decade, threshold voltage of −5 V, and maximum transconductance (g_m) of 100 nS. The mobility cannot be directly extracted because it is impossible to directly measure the effective channel width/length (W/L) due to the network path nature of the ZnO NWs. The SEM image [Fig. 3(c)] shows that the actual coverage with ZnO NWs is roughly below 20% and possibly below 5%. Assuming 100% coverage, effective field effect mobility (μ_{FE}) extracted from the I_d-V_g curve using the following relation[18] was around 0.2 $\mathrm{cm}^2/\mathrm{V\,s}$, which is comparable to the highest value reported for solution deposited and thermally annealed (700 °C) ZnO NP n-type FETs.[19]

$$\mu_{\mathrm{FE}} = \frac{g_m^2}{2I_d C_{\mathrm{ox}}(W/L)}.$$

The ZnO NWNT did not exhibit a clean saturation regime, which is possibly due to the increased carrier scattering by the complex NW network path, large surface area, and grain boundaries at NW junctions. Gao *et al.*[20] discussed the dominant phonon scattering and the impurity involved grain boundaries in bridged ZnO NWs across trenched electrodes. The complex NW networks connecting the source and drain electrodes are composed of numerous slanted 1–3 μm NWs connected together by forming junctions during the NW growth, as shown in Fig. 3(d). Since each NW has its own crystalline domain, the complete NW path that is composed of several NWs acts as a polycrystalline semiconductor. In addition, the associated electrostatics could be poor since some portions of the NWs lie further away from the gate and therefore experience less modulation, and large barrier is expected to exist between gold and ZnO.

To check the reproducibility of the current process, the yield statistics for the 400 transistors on two kinds of substrates (sample A, SiO_2/Si wafer; sample B, PVP/Al/PI substrate) were studied [Fig. 4(b)]. The ZnO NWNTs showed good yields for 6–20 μm channels for both rigid (sample A) and flexible (sample B) substrates. Both short channel (<6 μm) and long channel (>20 μm) showed a poor current on/off ratio with a large leakage current due to short channel effect and poor electrostatics, respectively.

In summary, we have successfully demonstrated all-solution processed, low-temperature ZnO NW transistor fabrication on polymer substrates by combining (1) source-drain electrode fabrication by direct nanoimprinting of metal NP solution and (2) the ZnO NW network synthesis by simple hydrothermal approach in water. This simple process can produce high resolution metal contact transistors with inorganic semiconductor NW in a fully maskless process, eliminating the need for microfabrication based on lithographic and vacuum processes. The temperature throughout the processing was below 140 °C, which will enable further applications to electronics on low-cost, large-area flexible polymer substrates.

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