# Palladium nanoparticle decorated silicon nanowire field-effect transistor with side-gates for hydrogen gas detection

Jae-Hyuk Ahn,[1,2,3] Jeonghoon Yun,[1,2,3] Yang-Kyu Choi,[4] and Inkyu Park[1,2,3,a)]
[1]*Department of Mechanical Engineering, KAIST, Daejeon 305-701, South Korea*
[2]*KI for the NanoCentury, KAIST, Daejeon 305-701, South Korea*
[3]*Mobile Sensor and IT Convergence (MOSAIC) Center, KAIST, Daejeon 305-701, South Korea*
[4]*Department of Electrical Engineering, KAIST, Daejeon 305-701, South Korea*

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A silicon nanowire field-effect transistor (SiNW FET) with local side-gates and Pd surface decoration is demonstrated for hydrogen ($H_2$) detection. The SiNW FETs are fabricated by top-down method and functionalized with palladium nanoparticles (PdNPs) through electron beam evaporation for $H_2$ detection. The drain current of the PdNP-decorated device reversibly responds to $H_2$ at different concentrations. The local side-gates allow individual addressing of each sensor and enhance the sensitivity by adjusting the working region to the subthreshold regime. A control experiment using a non-functionalized device verifies that the hydrogen-sensitivity is originated from the PdNPs functionalized on the SiNW surface. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4861228]

Hydrogen ($H_2$) sensors have been utilized in a wide range of industrial applications such as hydrogenation, petroleum refining processes, and hydrogen cooling system. Moreover, as $H_2$ has been considered as a strong candidate of future fuel and energy carrier, it increases the attention of $H_2$ sensors to be used in the fuel cell applications including leakage test and fuel monitoring.[1]

Palladium (Pd) has been widely used in the $H_2$ detection because of its high sensitivity and selectivity as well as room-temperature operation capability. Pd can absorb a large quantity of $H_2$ and be converted to palladium hydride ($PdH_x$) at room temperature. $H_2$ are dissociated on the Pd surface into hydrogen atoms, which then diffuse through the Pd layer and occupy the interstitial sites of the Pd lattice. The absorption/desorption of $H_2$ on the Pd surface are reversible and the coverage ($\theta$) of the absorbed hydrogen atoms is a function of partial pressure of $H_2$ ($P_{H_2}$) at equilibrium as following:[2]

$$\frac{\theta}{1-\theta} = \sqrt{\frac{k_a}{k_d} P_{H_2}}$$

where $k_a$ and $k_d$ are the absorption and desorption constants, respectively. The $H_2$ detection is based on the monitoring of the changes in electrical, mechanical, or optical properties of Pd.[1]

Because of simple structure and easy readout system, electrical sensors have been used for $H_2$ detection by monitoring the change in electrical properties of Pd upon the exposure to $H_2$. The electrical $H_2$ sensors include Pd thin films[3] and field-effect transistors (FET) with a Pd gate[4] to measure the resistivity and work function of Pd, respectively. To achieve high sensitivity, fast response, and low power consumption, researchers have been interested in using one-dimensional nanomaterials including Pd nanowires[5,6] and Pd nanotubes[7] as well as carbon nanotubes[8,9] and semiconducting nanowires[10,11] which are functionalized with Pd nanoparticles (PdNPs). These nanosensors are highly sensitive transducers that can convert the change of resistivity or work function of Pd into the large signals of current change.

Silicon nanowires (SiNWs) have various advantages over the other nanomaterials since they can be easily fabricated by well-developed complementary metal-oxide-semiconductor (CMOS) compatible process and the electrical properties of silicon can be easily modified by doping process.[12,13] There have been a few previous works on the $H_2$ sensors based on Pd-decorated SiNWs by using bottom-up synthesis[14] or top-down fabrication methods.[15] In this work, we would like to propose a SiNW FET-based $H_2$ sensor fabricated by top-down method, surface-functionalized with PdNPs and equipped with double gates for a field effect as shown in Figure 1(a). To complement two terminal SiNWs with a global bottom-gate, local side-gates are implemented beside the SiNW for multiple purposes such as individual addressing to each sensor in the array and sensitivity enhancement in $H_2$ detection by controlling the working region to the subthreshold regime in which a maximal sensitivity can be obtained.[16] Moreover, the proposed SiNW FET-based $H_2$ sensor shows a great potential in the mass production and commercialization because the fabrication process is similar to that of the FinFET, which has been recently commercialized in the Intel's microprocessor.[17]

The SiNW FETs were fabricated with previously reported top-down method.[18] As shown in Figure 2, the fabrication process was divided into two steps: fabrication of the SiNW (Figure 2(b)) and formation of the side-gates (Figure 2(d)). The SiNW was fabricated from a commercial silicon-on-insulator (SOI) wafer (SOITEC, p-Si(100) with a resistivity of 8.5–11.5 Ω·cm, a top silicon thickness of 55 nm, and a buried oxide thickness of 145 nm). A 80 nm thick silicon nitride layer was deposited on the SOI substrate by a low pressure chemical vapor deposition (LPCVD) method (Figure 2(a)). Later, the silicon nitride would be used as an etching stopper to protect the SiNW from being etched during chemical mechanical polishing (CMP) process

a)Author to whom correspondence should be addressed. Electronic mail: inkyu@kaist.ac.kr

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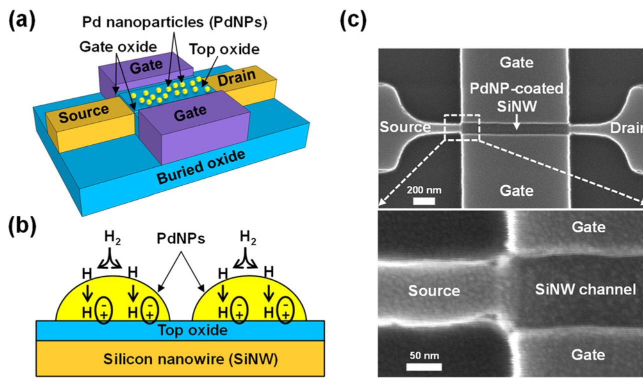


FIG. 1. Pd-decorated SiNW FET sensor with local side-gates: (a) Schematic of the SiNW FET for $H_2$ sensing. The SiNW FET is fabricated from a SOI substrate using a top-down process. Through metal evaporation, the SiNW is functionalized with PdNPs which are sensitive and selective to $H_2$ gas. The drain current is modulated by the two sidewall gates. The gates control the working region of the device from the linear to the subthreshold regime for the sensitivity improvement. (b) Schematic of the working principle of $H_2$ sensing in the Pd-decorated SiNW FET. The PdNPs dissociate $H_2$ into hydrogen atoms which diffuse into the PdNPs and generate hydrogen-induced dipole layers at the interface between PdNPs and the top oxide of the SiNW. The positive dipole layers lead to the change of the current through SiNW. (c) SEM images of the fabricated device. The top surface of the SiNW is decorated with PdNPs.

for the gate formation. Nanowire region was patterned by deep ultraviolet (DUV) lithography (KrF stepper; $\lambda = 248$ nm) and its pattern width was further reduced by photoresist ashing with oxygen plasma process. Then, the SiNW was fabricated by sequential dry etching of the silicon nitride and silicon layers (Figure 2(b)). As the first step to form the side-gates, a 5 nm thick silicon dioxide was grown as a gate oxide by thermal oxidation and a 200 nm thick $n^+$ *in situ* doped polycrystalline silicon (poly-Si) layer was deposited by LPCVD method as a gate electrode (Figure 2(c)). The protruding poly-Si layer was polished by the CMP process until the buried silicon nitride was exposed (Figure 2(d)). Thus, the top surface of the SiNW was opened and the sidewalls of the SiNW were covered by the remaining poly-Si layer. The gate region was formed by the DUV lithography and dry etching of the poly-Si. The silicon nitride layer

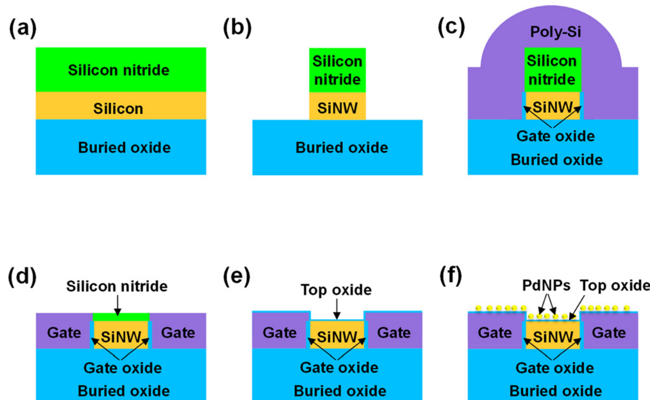


FIG. 2. Fabrication procedure of the Pd-decorated SiNW FET sensor with local side-gates: (a) deposition of the silicon nitride layer on the SOI wafer, (b) SiNW formation by photolithography and dry etching, (c) gate oxidation and LPCVD deposition of the poly-Si layer, (d) CMP of the poly-Si layer, (e) removal of the silicon nitride layer and thermal oxidation to produce the top oxide, and (f) surface decoration with the PdNPs by electron beam evaporation.

on the source/drain region was removed by the dry etching and ion implantation (Arsenic, energy of 30 keV and a dose of $5 \times 10^{15}$ cm$^{-2}$) was carried out to form self-aligned source/drain with the gate pattern as an implant mask. A process of rapid thermal annealing (1000 °C, 5 s) was performed to activate the dopants. The remaining silicon nitride was stripped out with hot phosphoric acid (150 °C, 20 min) to expose the silicon surface underneath the silicon nitride. A thin silicon oxide layer with a thickness of 3 nm was grown on top of the SiNW by thermal oxidation (Figure 2(e)). Finally, forming gas (10% $H_2$ + 90% $N_2$) annealing was performed at 400 °C for 30 min for stable operation of the devices by passivating dangling bonds with hydrogen atoms at the Si-$SiO_2$ interface.

For selective and sensitive detection of $H_2$ with the SiNW FET, the SiNW surface was functionalized with PdNPs by depositing a very thin film (thickness = ~1 nm) on the device using an electron beam evaporator (Figure 2(f)). It is well known that a very thin metal film (thickness < ~2 nm) is deposited on the oxide with a shape of nanoparticles instead of a continuous thin film because the metal atoms tend to agglomerate with each other due to the low surface energy of the oxide.[11]

Figure 1(c) shows the scanning electron microscopy (SEM) images of the PdNP-coated SiNW FET with a nanowire width of 100 nm and a gate length of 1 $\mu$m. The side-gates are formed at the sidewall of the SiNW and the PdNPs are deposited on the opened top surface of the SiNW, which serves as a sensing site to detect $H_2$ molecules. Although a global bottom-gate is commonly used in SiNW sensors,[14] the local gates of the fabricated devices can enable selective addressing to individual devices in a sensor array.

The transfer characteristics of the fabricated devices were measured by using a semiconductor parameter analyzer (HP 4156 C). The drain current was measured while the gate voltage was swept from −3 V to 2 V with a constant drain voltage of 50 mV. In this case, the two gates were electrically tied by using a T-shaped connector and thus the same voltage was applied to the gates ($V_{G1} = V_{G2}$) because the current response can be maximized in this condition as confirmed with a semiconductor device simulator.[19] In the simulation result, the cross-sectional distribution of the electron concentration reveals that two channels are formed symmetrically along the bottom corners of the SiNW under the symmetric bias condition ($V_{G1} = V_{G2}$). The current response is maximized because both of these two channels are involved in the electrostatic interaction with the top surface ($H_2$-sensitive layer). Under the asymmetric bias condition ($V_{G1} \neq V_{G2}$), however, larger amount of electrons are concentrated near the single bottom corner of the SiNW close to the side-gate with higher voltage and thus the asymmetric channel is formed. In this case, the electrostatic interaction between the top surface and the channel is reduced and the current response is also degraded.

As shown in Figure 3(a), the fabricated devices show n-type FET characteristics with high on/off ratio over $10^5$. The good controllability of the current level with the gates implies that the electron concentration inside the SiNW can be well adjusted, which underlies the sensitivity improvement of the sensor that will be investigated below. The effect of surface

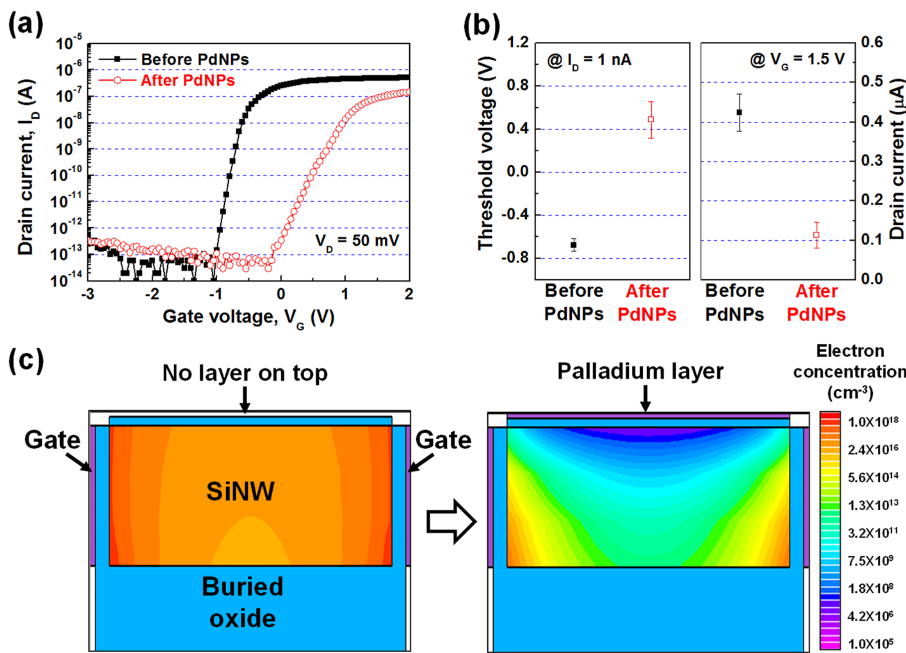


FIG. 3. Electrical characteristics and cross-sectional distribution of electron concentration of the Pd-decorated SiNW FET sensor before and after the PdNP decoration: (a) Transfer ($I_D$-$V_G$) characteristics, (b) Threshold voltage and drain current; The threshold voltage is defined as a gate voltage at the drain current of 1 nA. The drain current is read at the gate voltage of 1.5 V. (c) Simulated electron concentration under zero bias of side-gates ($V_{G1} = V_{G2} = 0$ V) before and after setting the palladium layer (top gate) with a work function of 5 eV on the top surface.

modification with PdNPs on the electrical characteristics of the SiNW FETs was investigated. To avoid the misunderstanding from device-to-device variation, the same device was used in the Pd deposition and the electrical characterization. Figure 3(a) shows that the $I_D$-$V_G$ curve is shifted toward the right-hand side after the deposition of the PdNPs. It is worthwhile to note that the off-state leakage current is not changed by the deposition of PdNPs on the device. This result implies that a current path is not created via the PdNP thin film and thus the PdNPs are only involved in the surface functionalization of the SiNW. As shown in the statistical data of Figure 3(b), the threshold voltage increases and the drain current decreases after the decoration of the PdNPs. The changes of the electrical characteristics are consistent with previous reports regarding n-type semiconducting nanowire FETs.[10,11,14] The cross-sectional electron density was extracted from the simulation to study how the PdNPs affects the channel inside the SiNW. As shown in Figure 3(c), the electrons near the top surface are depleted after setting the palladium layer (top gate) due to high work function of the palladium (5 eV), which leads to the changes of the electrical characteristics. Then, the channels are formed on the bottom corners of the SiNW while overall electrical conductance is decreased.

For the $H_2$ sensing experiments, the fabricated devices were mounted on a custom-built chamber probe station in which electrical probing system was constructed and a gas inlet/outlet was connected. The test $H_2$ gas was injected into the gas inlet by mixing of 1% $H_2$ gas and background air from gas cylinders. The concentration of the test $H_2$ gas was changed by controlling the flow rates of each gas using mass flow controllers (MFCs) while the total gas flow rate was maintained at 300 sccm. The real-time measurement of the drain current was performed by using a dual-channel source meter (Keithely 2636B) under a constant drain voltage of

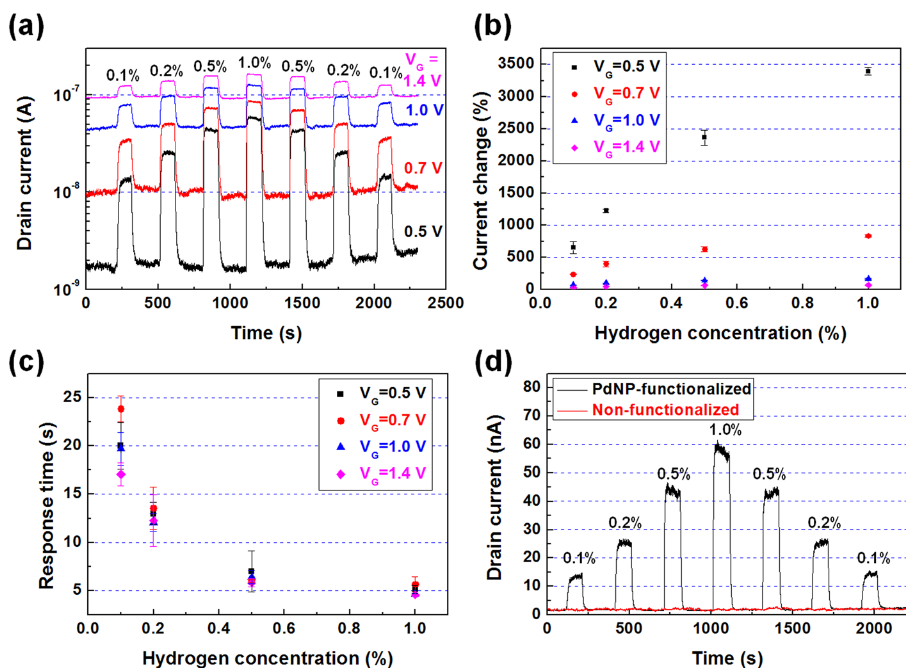


FIG. 4. $H_2$ sensing characteristics of the Pd-decorated SiNW FET sensor: (a) Real-time measurement of the drain current upon the exposure to $H_2$ with different concentrations under various gate voltages, (b) Effect of the gate voltage on the detection sensitivity; the sensitivity is dramatically improved by operating at the subthreshold regime ($V_G = 0.5$ V) as compared to the linear regime ($V_G = 1.4$ V). (c) Response times at different $H_2$ concentrations, (d) Control experiment through comparison of non-functionalized device with the PdNP-functionalized device upon the $H_2$ exposure

TABLE I. Comparison table of sensor performance with previous one-dimensional nanomaterial based sensors.

| Sensor specification | $H_2$ concentration (%) | Sensitivity (%) | Response time (s) | References |
|---|---|---|---|---|
| PdNP-decorated SiNW FET (W = 100 nm, T = 50 nm, L = 1 $\mu$m) | 0.5 | 2360 | 7 | This work |
| Pd nanowire (W = 93 nm, T = 11 nm, L = 106 $\mu$m) | 0.5 | 10 | 40 | 6 |
| Pd nanotube (D = 50–100 nm, L = 1–2 $\mu$m) | 0.5 | 1800 | 80 | 7 |
| PdNP-decorated InAs nanowire (W = 360 nm, T = 8 nm, L = 2.5 $\mu$m) | 0.5 | 200 | N/A | 11 |
| PdNP-decorated SiNW (D = 80–200 nm, L = 4 $\mu$m) | 5.0 | 1900 | 2 | 14 |

50 mV and a fixed gate voltage with various conditions. The MFCs and the source meter were controlled by a computer using a GPIB interface and LabView software. All experiments were performed at room temperature.

As shown in Figure 4(a), the drain current is increased upon the injection of the $H_2$ gas but reduced again after the injection of fresh air. When the concentration of the $H_2$ gas is increased from 0.1% to 1%, the drain current is also increased according to the concentrations. As depicted in Figure 1(b), hydrogen atoms dissociated on the surface of the PdNPs diffuse through the Pd layer and are absorbed onto the Pd-$SiO_2$ interface on top of the SiNW. Then, these hydrogen atoms are polarized and give rise to a positive dipole layer,[4] which increases the drain current by attracting electrons flowing through the SiNW. The drain current is reduced again by decreasing the $H_2$ concentrations from 1% to 0.1%, which confirms the reversibility of the fabricated device.

The effect of the working regime (from subthreshold to linear regime) on the sensitivity to detect the $H_2$ gas was investigated by measuring the drain current under conditions of different gate voltages. Here, the sensitivity of the SiNW was defined by $S = (I_{H2} - I_{air})/I_{air} \times 100$ (%) where $I_{air}$ and $I_{H2}$ are the drain currents of the PdNP-functionalized SiNW in air and in $H_2$, respectively. As shown in Figures 4(a) and 4(b), the sensitivity is enhanced when the device is operated in the subthreshold regime ($V_G = 0.5$ V) but it is suppressed as the gate voltage is increased and reached to the linear regime ($V_G = 1.4$ V). The sensitivity in the subthreshold regime was measured to be 3400% at 1% $H_2$ concentration, which is $\sim$50 times higher than the sensitivity measured in the linear regime. As shown in the transfer characteristics of Figure 3(a), the drain current is exponentially changed by the gate voltage at the subthreshold regime, whereas the drain current is linearly varied at the linear regime. By modulating the working regime of the device to the subthreshold regime using the side-gates, the drain current exponentially responds to an additional top gate voltage (i.e., positive dipole layer by the polarized hydrogen atoms), thereby the sensitivity can be improved. This result is also consistent with previous work by Nair *et al.* in which high percentage response was shown in a low electron concentration condition (i.e., subthreshold regime) as compared to a high electron concentration condition (i.e., linear regime).[20] As shown in Figure 4(c), when the $H_2$ concentration is increased form 0.1% to 1.0%, the response time defined as the time interval between 10% and 90% increment of the sensor signal, is reduced from 24 to 5 s. The response time is independent of the gate voltage and thus the sensitivity can be improved by modulating the working regime without sacrificing the response time. As summarized in Table I, the $H_2$ sensitivity and response time of our Pd-decorated SiNW FET-based $H_2$ sensor is comparable or higher than those of other one-dimensional nanomaterial based sensors.[6,7,11,14] It is expected that the high sensitivity and fast response time of our sensor are due to the effective modulation of the carrier density inside the SiNW using the side-gates as well as the rapid reaction of the thin layer of the PdNPs decorated on the SiNW upon the $H_2$ exposure.

A control experiment using the non-functionalized SiNW FET was conducted to assess the effect of the surface functionalization with the PdNPs on the detection of the $H_2$ gas. As shown in Figure 4(d), no response upon the $H_2$ exposure is observed in various $H_2$ concentrations, which implies that non-functionalized SiNWs have no reactivity with $H_2$ gas. Therefore, it is confirmed that the notable change of the drain current upon the $H_2$ exposure originates from the functionalization of SiNW surface with the PdNPs.

In conclusion, SiNW FETs with the local side-gates were fabricated from the SOI wafer using top-down method that was used in the fabrication of commercial FinFETs, and functionalized with the PdNPs by evaporation of a thin Pd film to be used for the detection of $H_2$ gas. The drain current of the PdNP-functionalized device was changed upon the $H_2$ exposure and returned to the original level after air flushing. The non-functionalized device showed no response to $H_2$ exposure, implying that the $H_2$-sensitive characteristics were caused by the PdNPs decorated on the SiNW surface. The drain current of the PdNP-functionalized device properly responded to various $H_2$ concentrations. Implementation of the local side-gates beside the SiNW provided not only the individual access to each sensor but also the enhancement of sensing performance. By modulating the gate voltage with the side-gates, the sensitivity was dramatically enhanced since the sensor could be operated in the subthreshold regime. As explained above, the most significant advantage of this technology is that the device can be mass-manufactured with low cost by using well-established IC microfabrication processes. It is expected that the Pd-decorated SiNW FET sensors with local side-gates will be very promising devices for the highly sensitive detection of $H_2$ gases in various applications such as hydrogen conversion, storage and power generation systems.

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